Do FPGA designers and hardware designers need to talk?

A practical approach to shortening the project timeline.

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Who am I?

15 years of FPGA experience:

commercial (Ericsson, GE, Arrow, Brightelligence)

scientific

- ✔ Lodz University of Technology, Poland
- ✔ Gdansk University of Technology, Poland
- ✔ Military University of Land Forces, Poland
- ✔ Nicolaus Copernicus Astronomical Center, Poland
- ✔ Universitat Politècnica de Catalunya, Spain
- ✔ University of Glasgow, Scotland
- ✔ University of Trento, Italy

Goal

Get all your questions answered.

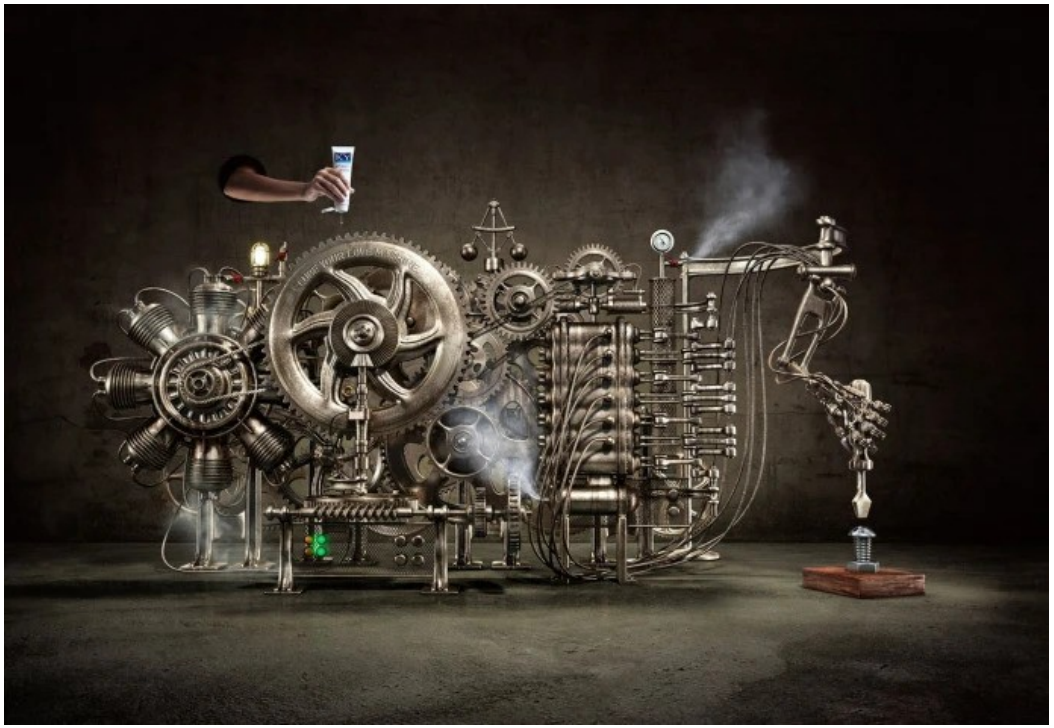
Be a little wiser after the session.

Who should be responsible for selection of the FPGA?

Who should be responsible for selection of the FPGA?

It depends.

- Large / small company
- Experience
- Budget



System architect

System engineer

Hardware engineer

FPGA engineer

When should engineers start cooperating?

When should engineers start cooperating?

As soon as the project starts.

8 months

PN selected

Everything fits

interface	V1	V2	V3	V4	V5
I1				√	√
I2	√		√		√
I3	√		√		√
I4			√	√	√
I5		√		√	√
I6		√		√	√

Kamil: No, it doesn’t.

Who should be responsible for I/O placement?

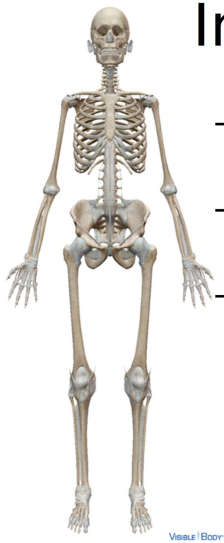
Who should be responsible for I/O placement?

It depends.

- large / small company
- experience
- project / chip complexity
- performance

In ideal case scenario:

- system engineer selects
- hardware engineer helps
- FPGA engineer verifies



GTY Quad 133 X0Y36-X0Y39 S [LN]	CMAC X0Y5	HP I/O Bank 53	HP I/O Bank 73	ILKN X1Y5	GTY Quad 233 X1Y36-X1Y39 J [RN]
GTY Quad 132 X0Y32-X0Y35 R [LN]	PCIE4 X0Y3	HP I/O Bank 52 L	HP I/O Bank 72 O	ILKN X1Y4	GTY Quad 232 X1Y32-X1Y35 I [RN]
GTY Quad 131 X0Y28-X0Y31 Q [LN] (RCAL)	CMAC X0Y4	HP I/O Bank 51 K	HP I/O Bank 71 N	SYSMON Configuration	GTY Quad 231 X1Y28-X1Y31 H [RN] (RCAL)
GTY Quad 130 X0Y24-X0Y27 P [LN]	ILKN X0Y3	HP I/O Bank 50 J	HP I/O Bank 70 M	Configuration	GTY Quad 230 X1Y24-X1Y27 G [RN]
GTY Quad 129 X0Y20-X0Y23 O [LN]	CMAC X0Y3	HP I/O Bank 49	HP I/O Bank 69	PCIE4 X1Y2	GTY Quad 229 X1Y20-X1Y23 F [RN]
SLR Crossing					
GTY Quad 128 X0Y16-X0Y19 N [LS]	CMAC X0Y2	HP I/O Bank 48	HP I/O Bank 68 F (Partial)	ILKN X1Y2	GTY Quad 228 X1Y16-X1Y19 E [RS]
GTY Quad 127 X0Y12-X0Y15 M [LS]	PCIE4 X0Y1	HP I/O Bank 47	HP I/O Bank 67 E	ILKN X1Y1	GTY Quad 227 X1Y12-X1Y15 D [RS]
GTY Quad 126 X0Y8-X0Y11 L [LS] (RCAL)	CMAC X0Y1	HP I/O Bank 46 I	HP I/O Bank 66 D	SYSMON Configuration	GTY Quad 226 X1Y8-X1Y11 C [RS] (RCAL)
GTY Quad 125 X0Y4-X0Y7 K [LS]	ILKN X0Y0	HP I/O Bank 45 H	HP I/O Bank 65 C	Configuration	GTY Quad 225 X1Y4-X1Y7 B [RS]
GTY Quad 124 X0Y0-X0Y3	CMAC X0Y0	HP I/O Bank 44 G	HP I/O Bank 64 B	PCIE4 X1Y0 (tandem)	GTY Quad 224 X1Y0-X1Y3 A [RS]

X16504-020817

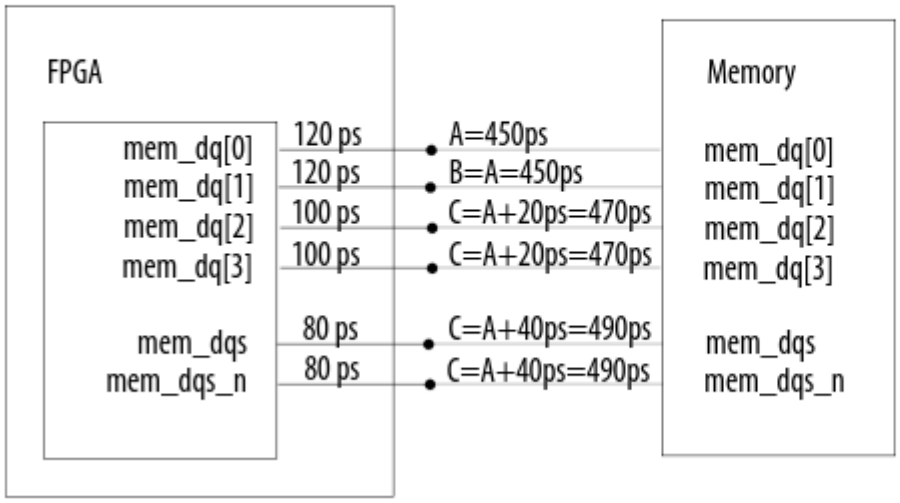
Figure 1-111: **XCVU5P Banks in FLVB2104 Package**

Is package deskew an important topic?

Is package deskew an important topic?

It can be.

Figure 73. Figure 97. Deskew Example with Trace Delay Calculations



Protocol	Minimum Frequency (MHz) for Which to Perform Package Deskew		
	Single Rank	Dual Rank	Quad Rank
DDR4	933	800	667
DDR3	933	800	667
LPDDR3	667	533	Not required
QDR IV	933	Not applicable	Not applicable
RLDRAM 3	933	667	Not applicable
QDR II, II+, II+ Xtreme	Not required	Not applicable	Not applicable

Who should be responsible for constraints?

Who should be responsible for constraints?

FPGA engineer must have/use it.

In ideal case scenario:

- hardware engineer specifies them
- FPGA engineer verifies them

```
IOBUF PORT "pi_m_2_config[1]" IO_TYPE=LVCMOS33 ;
IOBUF PORT "pi_m_2_config[2]" IO_TYPE=LVCMOS33 ;
IOBUF PORT "pi_m_2_config[3]" IO_TYPE=LVCMOS33 ;
LOCATE COMP "pi_pwr_good_5v" SITE "R16" ;
LOCATE COMP "pi_pwr_good_3v3" SITE "P15" ;
LOCATE COMP "pi_pwr_good_eth_sw_phy" SITE "N14" ;
LOCATE COMP "pi_pwr_good_cpld" SITE "N16" ;
LOCATE COMP "pi_pwr_good_pcie_0v8" SITE "P16" ;
LOCATE COMP "pi_pwr_good_pcie_1v8" SITE "M15" ;
```

Who should be responsible for naming I/Os?

Who should be responsible for naming I/Os?

1) HW engineer

+ Hardware engineer may generate constraints file.

- The names may not fit your notation.

2) FPGA engineer

+ The names fit your notation.

- A change in the signal use may not be reflected in the name.

3) hybrid

Is jitter consideration important?

Is jitter consideration important?

Yes, it is. Who is responsible for this?

Hardware engineer takes care of that.

- FPGA engineer verifies that.

Who should be responsible for selection of the ARM parameters during bring-up?

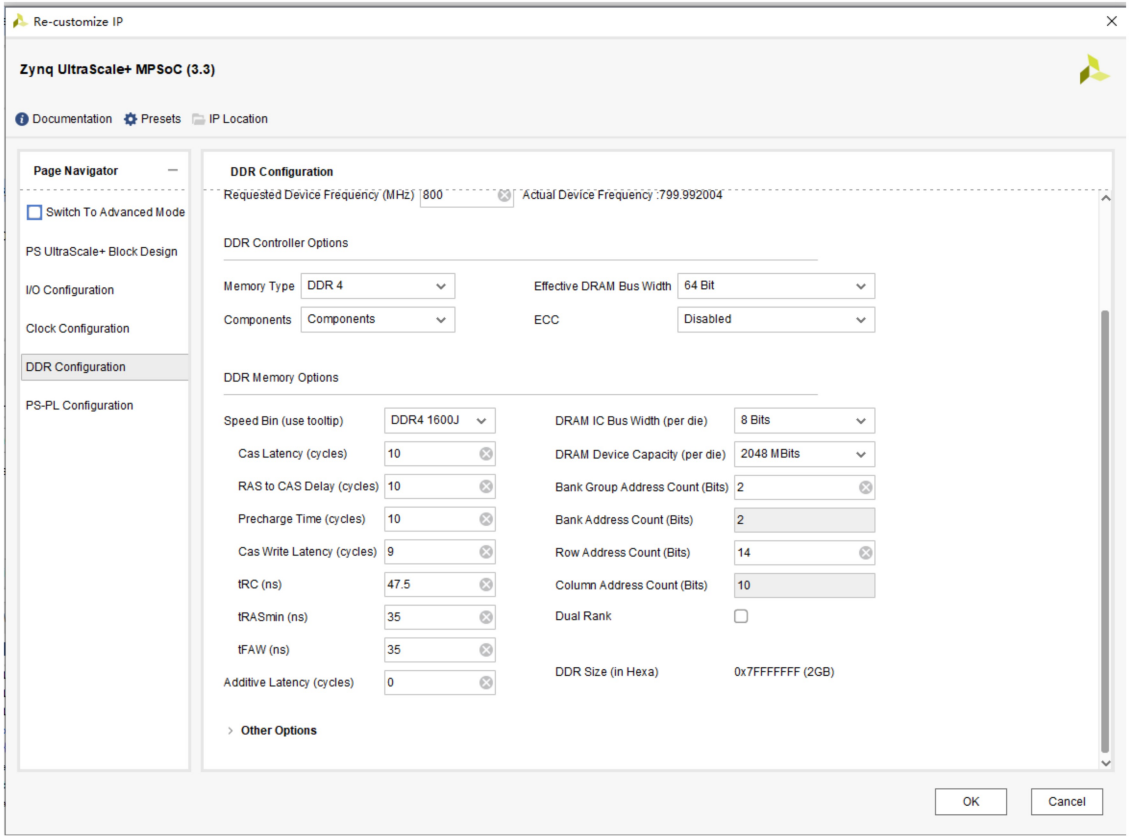
Who should be responsible for selection of the ARM parameters during bring-up?

Hardware engineer.

With help from

FPGA engineer

software engineer



Who is responsible when something doesn’t work?

Who is responsible when something doesn’t work?

FPGA engineer.

With help from

hardware engineer

software engineer

100G Ethernet

IP replacement

How should we communicate?

How should we communicate?

Document everything.

I2C

GPIO

Thank you.